Drawing Amendments

Please replace the number of the steps in Figure 3 as follows:

Replace "51" with "S1";

Replace "52" with "S2";

Replace "53" with "S3";

Replace "54" with "S4";

Replace "55" with "S5";

Replace "56" with "S6";

Remarks

Thorough examination by the Examiner is noted and appreciated.

The drawings have been amended to reflect item numbering consistent with the Specification.

The Specification has been amended to correct grammatical errors and reflect numbering consistent with the drawings.

The claims have been amended and new claims added to clarify Applicants disclosed and claimed invention and to correct grammatical errors as suggested by Examiner. The amendments find support in the original claims and/or the Specification. No new matter has been added. For example support for amendments to the independent claims 1, 9, and 15 as well as dependent claim 8 and new claims 26 and 27 is found in the original claims and in the Specification at the paragraphs below and Figure 2E:

at paragraph 0052:

"As further shown in Figure 1B, **a problem which frequently results in the etching of the polysilicon layer 16 using a chlorine-based etchant gas** mixture is that a neck 17 forms in the upper end portion of the polysilicon layer 16. **This necking or notched profile is undesirable** since optimum semiconductor fabrication requires that the sidewalls 16a of the etched polysilicon layer 16 be as straight and uniform as possible."

and at paragraph 0059:

"Still another object of the present invention is to provide a novel polysilicon gate fabrication method which may include etching of a polysilicon layer using a **fluorine-based etchant gas** followed by etching of the polysilicon layer using a **non-fluorine-based etchant gas** to eliminate or at least substantially reduce the tendency to form a necking profile in the polysilicon layer."

and at paragraph 0061:

"In accordance with the present invention, the polysilicon layer may be etched according to a **two-step etch process**. In the first etching step, the polysilicon layer is partially etched using a fluorine-based etchant gas. In the second etching step, etching of the polysilicon layer is completed using a non-fluorine-based etchant gas. The non-fluorine-based etchant gas may be an etchant gas mixture which includes chlorine, oxygen, helium and bromine, for example."

and paragraph 0067:

After fabrication of the multi-layered semiconductor structure, the hard mask layer is etched according to the patterned resist layer. The resist layer is then stripped from the mask layer. The polysilicon layer is then etched according to the mask layer, an etchant gas mixture which includes fluorine. The **fluorine-based etching process** imparts a substantially uniform sidewall profile, which is substantially **devoid of a necking or notched configuration**, to the etched polysilicon gate layer.

and at paragraphs 0079-0080:

"Referring next to Figure 2E and step S5 of Figure 3, in the partial-etch step, a fluorine-based gas **is used to partially etch the polysilicon layer 36** according to the pattern defined by the patterned and etched hard mask layer 38. The fluorine-based etching process is typically carried out in a high density plasma (HDP) etch chamber. **The fluorine-based etchant gas may include a gas such as fluorocarbon, fluoronitride or fluorosulfur, in non-exclusive particular.** Application of the fluorine-based etchant gas in the partial etch step is typically followed by the complete etch step, **which utilizes an etchant gas devoid of fluorine and typically having chlorine, bromine, oxygen and helium** to enhance etching profile uniformity in the sidewalls of the etched polysilicon layer 36.

Typical process parameters for the fluorine-based partial-etch step S5 include a chamber pressure of typically from about 5 mTorr to typically about 80 mTorr; a source radio frequency of from typically about 100 watts to about 1500 watts at a source radio frequency of 13.56 MHz; a bias power of from typically about 50 to typically about 1500 watts; **and a fluorine-based etchant gas flow rate of typically about 100 sccm.**"

Claim Rejections under 35 USC 112

Claim 6, 8, 10, 13, 16, and 20-22 stand rejected under 35 USC 112, second paragraph. The claims have been amended to overcome Examiners rejections.

U.S.S.N. 10,804,449

Claim Rejections under 35 USC 102

1. Claims 1-2, 4, 6-10, and 13 stand rejected under 35 USC Section 102(b) as being anticipated by Kumar et al. (US 5,851,926).

Kumar et al. disclose a method for etching a polysilicon gate using an etch chemistry including nitrogen trifluoride and chlorine (Cl2) (see col 2, lines 26 to 34), preferably including HBr, nitrogen, or oxygen as a sidewall passivant in a single polysilicon etch step. Kumar et al. also teach an **overetch process** following endpoint detection of an underlying gate oxide (after etching through a thickness of the polysilicon in a single step) to remove all material over the gate oxide (col 3, lines 11-17). Specifically, Kumar et al. disclose and teach a **chlorine and fluorine** based etch chemistry disclosed as **75 to 85 vol% chlorine** (Cl_2) and 15 to 25 vol% NF_3, (col 3, lines 66 to col 4, line 2); or 75 to 80 vol% chlorine (Cl_2) and 10 to 15 vol% NF_3, and 5 to 10 vol% HBr. Kumar et al. disclose examples of etching chemistries in Example 1 for the **chlorine and fluorine based etching chemistry** including two **control etch examples** including a similar amount of chlorine (Cl_2) and fluorine in the form of SF6 (col 4, lines 50-53) in addition to HBR; col 5, lines 1-7.

Thus, Kumar et al. do not teach or disclose several elements of Applicants claimed invention including:

"partially etching through a first thickness of said silicon layer according to said hard mask layer without exposing the underlying substrate using a fluorine based etching chemistry consisting primarily of a fluorine containing etchant gas; and,

then etching through a remaining thickness of said silicon layer to expose said underlying substrate according to said hard mask layer using an etchant gas devoid of fluorine."

Rather, Kumar et al. disclose a single step etching process which can be characterized as a **chlorine based etching chemistry (75 to 85 vol% chlorine (Cl_2)**. Kumar et al. **do not** disclose Applicants two-step etch process for etching the silicon layer including the second etch step devoid of fluorine as Applicants have disclosed and claimed, but rather disclose **an overetch process** following endpoint detection (complete etching through the silicon layer thickness to expose the underlying gate oxide(substrate) where the overetch process is a chlorine base based etching chemistry (devoid of fluorine) using a HBr, Cl_2, oxygen, and helium (col 4, lines 29-33).

Thus, Kumar et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. Claims 1, and 5-8 stand rejected under 35 USC Section 102(e) as being anticipated by Chan et al. (US 6,828,237).

Chan et al. disclose a multiple step etching process where a silicon layer is etched through a first thickness according to a hardmask which forms an etch residue alongside the mask thereby increasing the dimensions of the hardmask; **the hardmask is then removed followed by a second etching step** through a second thickness portion of the silicon layer which is then followed by a **third etching step** to etch through a remaining thickness of the silicon layer (see Abstract; col 2 lines 12-21).

Thus, Chan et al. is also clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103

1. Claims 3, 5, 12, and 14 stand rejected under 35 USC Section 103(a) as being unpatentable over Kumar et al., above.

Applicants reiterate the comments made above with respect to Kumar et al.

Further, with respect to claims 3 and 14, Applicants note that since Kumar et al. do not disclose Applicants **two-step** etching process for etching through a silicon thickness, the recitation of *In re Aller* to the claimed etching conditions is inapplicable.

With respect to claims 5 and 12 (and 19), the fact that Examiner takes **official notice** that using a pre-doped polysilicon layer is conventional or well-known in the art does not help Examiner establish a *prima facie* case of obviousness.

"A statement that modifications of the prior art to meet the claimed invention would have been "`well within the ordinary skill of the art at the time the claimed invention was made'"

because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

Examiner provides no teaching or suggestion for the notion that Applicants etching process together with the doping condition of the polysilicon layer would be desirable or could successfully solve the problem that Applicants have identified and solved by their disclosed and claimed invention: "A method for forming a patterned silicon-containing structure to avoid notching along sidewalls of said structure".

Moreover, Kumar et al. do not disclose or suggest a **two step etch process** as Applicants have disclosed and claimed, **but rather**

disclose a single etch process followed by an overetch process i.e., following partial exposure of the gate oxide (substrate). In addition, Kumar et al. **teach away** from Applicants disclosed and claimed invention by teaching a **chlorine and fluorine based etching chemistry (primarily consisting of chlorine)** in the disclosed single silicon etching step to etch through the entire thickness of the silicon layer. The method of Kumar et al. therefore represents the very conditions bringing about the problem that Applicants have recognized in the prior art, and solved by their disclosed and claimed invention. See e.g., paragraph 0052 of Applicants disclosure:

"As further shown in Figure 1B, **a problem which frequently results in the etching of the polysilicon layer 16 using a chlorine-based etchant gas mixture** is that a neck 17 forms in the upper end portion of the polysilicon layer 16. This necking or notched profile is undesirable since optimum semiconductor fabrication requires that the sidewalls 16a of the etched polysilicon layer 16 be as straight and uniform as possible."

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

2. Claims 11, and 15-22 stand rejected under 35 USC Section 103(a) as being unpatentable over Kumar et al., above, and further in view of Tao et al. (6,156, 629).

Applicants reiterate the comments made above with respect to Kumar et al.

Tao et al. disclose a three step etch process for first etching through the BARC layer and the hardmask layer, then in-situ stripping the BARC layer, and then followed **by a single etch process to etch through the silicon (poly or amorphous) layer** using a **bromine and chlorine based etch chemistry** (col 6, lines 19-27; col 8, lines 33-67; Table 3).

Assuming *arguendo*, a proper motivation for combining the teachings of Kumar et al. and Tao et al., such combination fails to produce Applicants disclosed and claimed invention, but rather presents the very conditions that Applicants disclosed and claimed invention solves. Thus, Kumar et al. and Tao et al., either singly or in combination, are insufficient to make out a *prima facie* case of obviousness.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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